# FIGURE 1

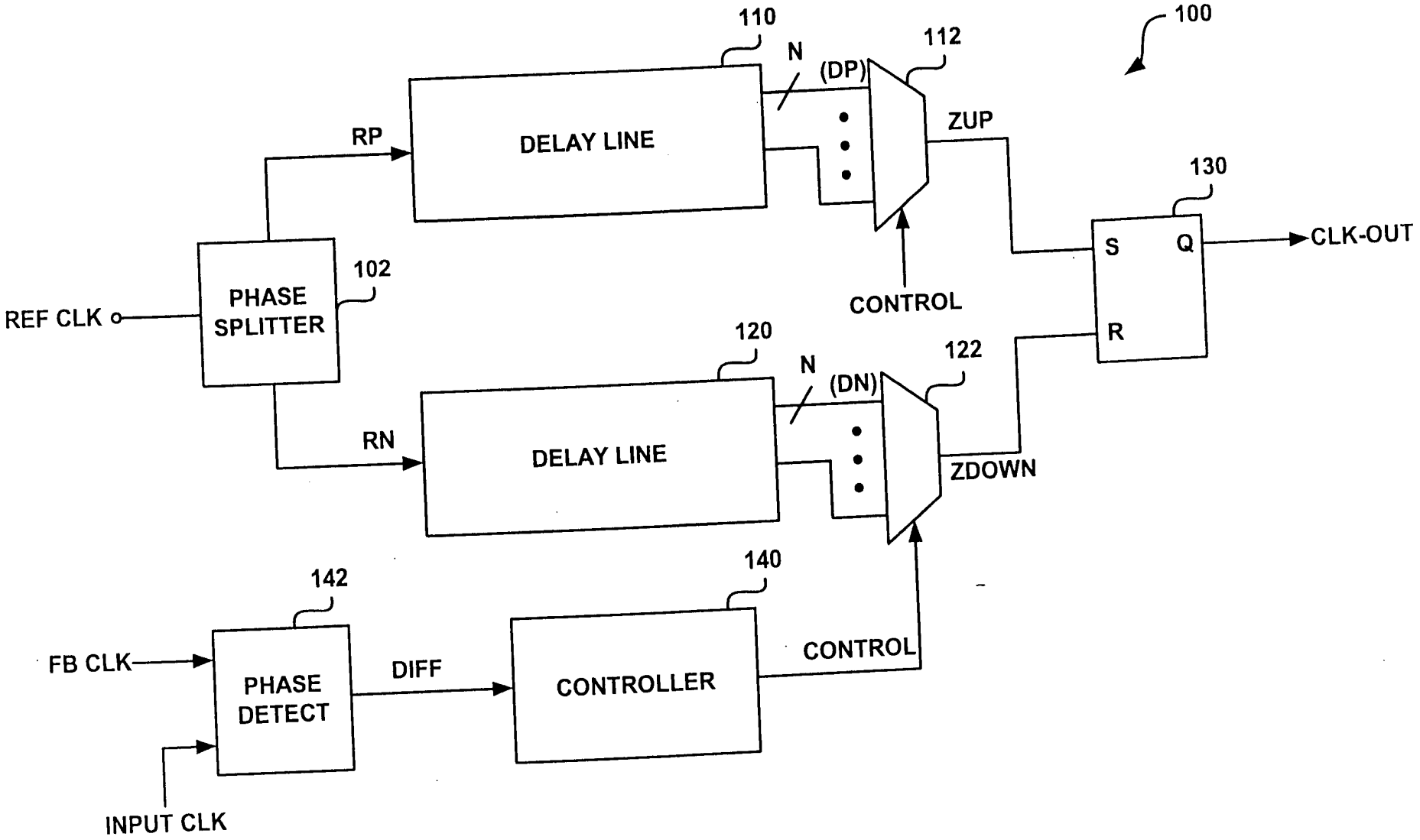
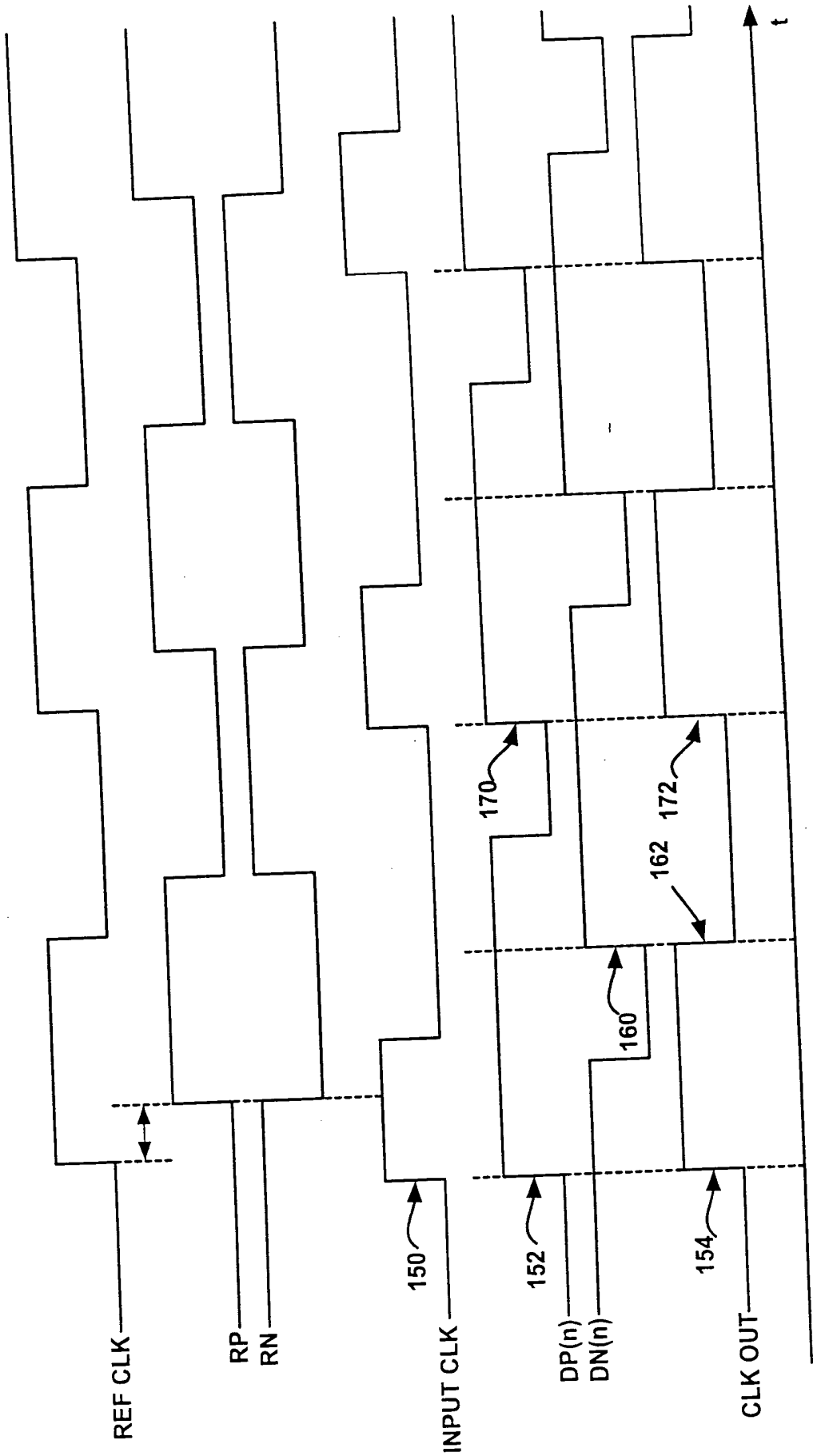

100
110
N
(DP)
112
RP
DELAY LINE
ZUP
130
S
Q
CLK-OUT
REF CLK
PHASE SPLITTER
102
CONTROL
R
120
N
(DN)
122
RN
DELAY LINE
ZDOWN
140
142
FB CLK
PHASE DETECT
DIFF
CONTROLLER
CONTROL
INPUT CLK

FIGURE 2


REF CLK
RP
RN
150
INPUT CLK
152
DP(n)
DN(n)
154
CLK OUT
170
172
162
160
t

# FIGURE 3

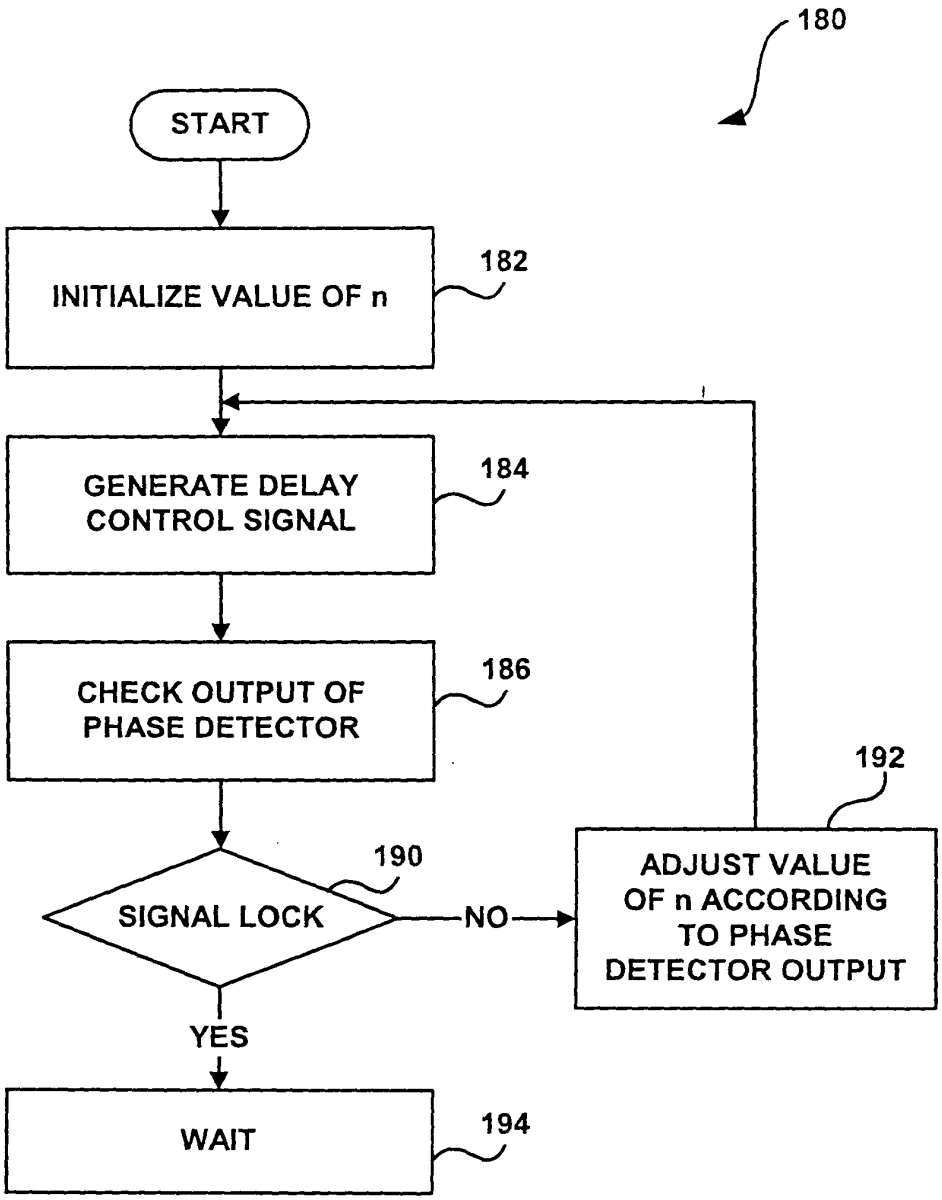
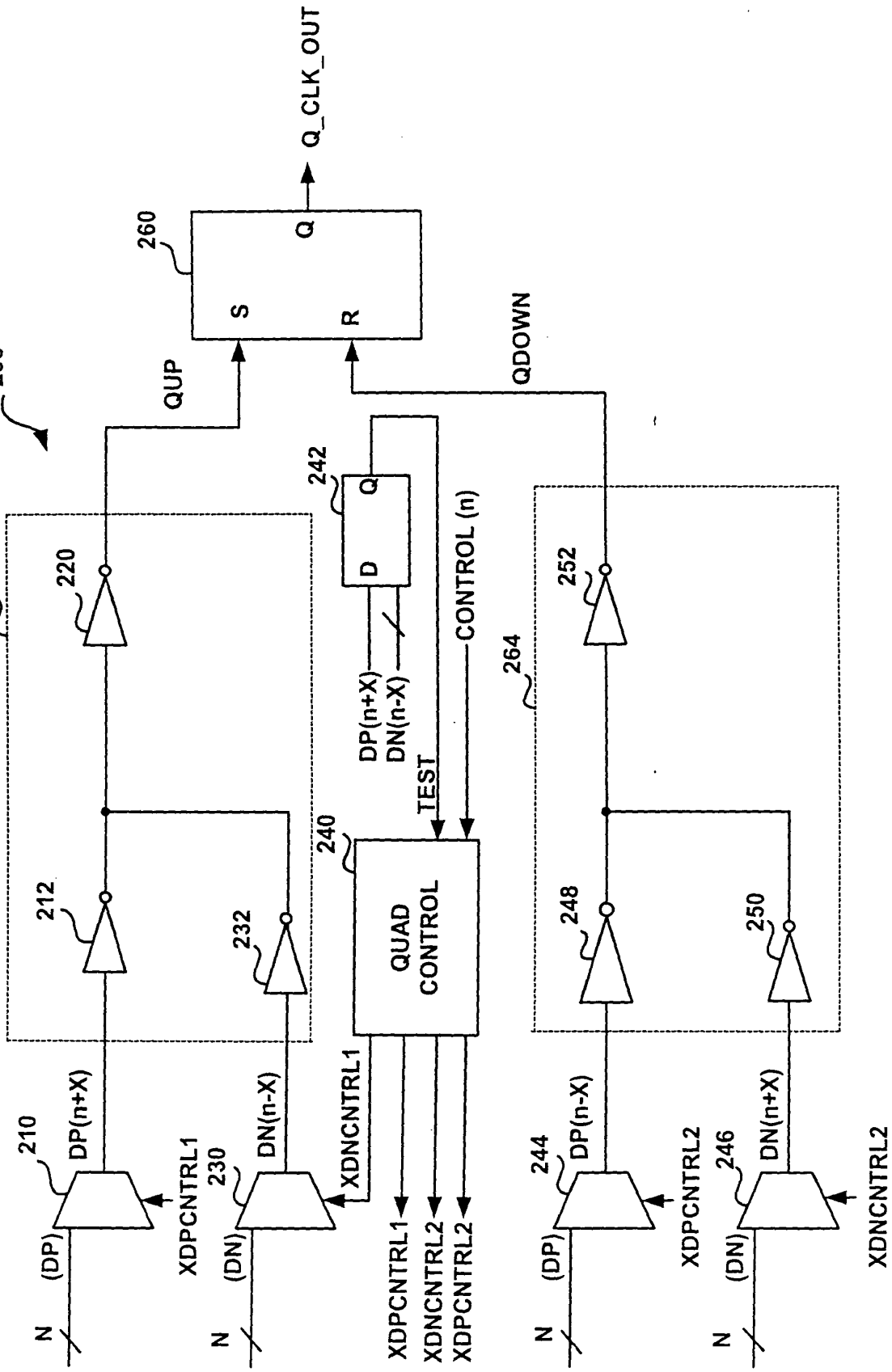
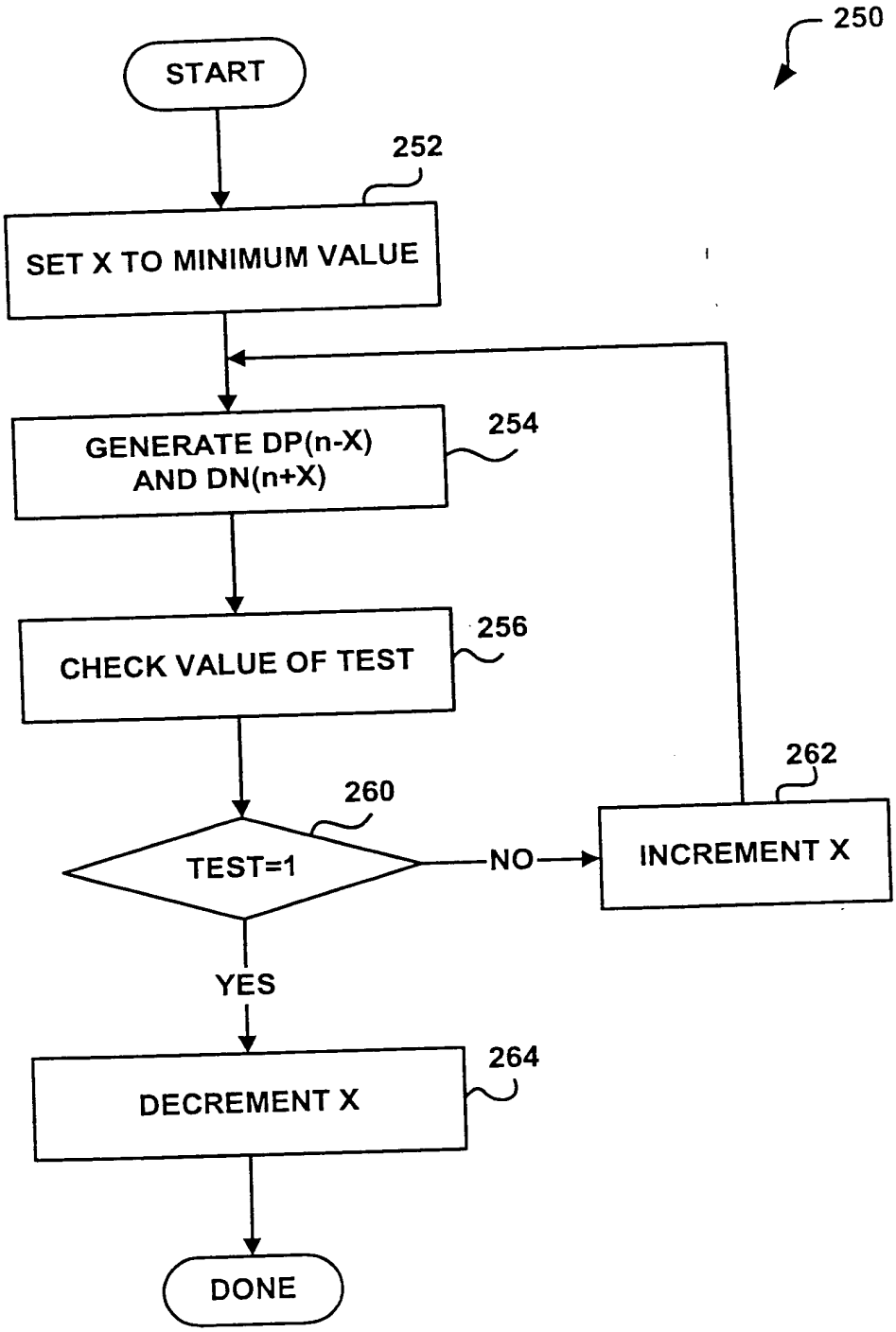

180
START
INITIALIZE VALUE OF n
182
GENERATE DELAY CONTROL SIGNAL
184
CHECK OUTPUT OF PHASE DETECTOR
186
SIGNAL LOCK
190
NO
ADJUST VALUE OF n ACCORDING TO PHASE DETECTOR OUTPUT
192
YES
WAIT
194

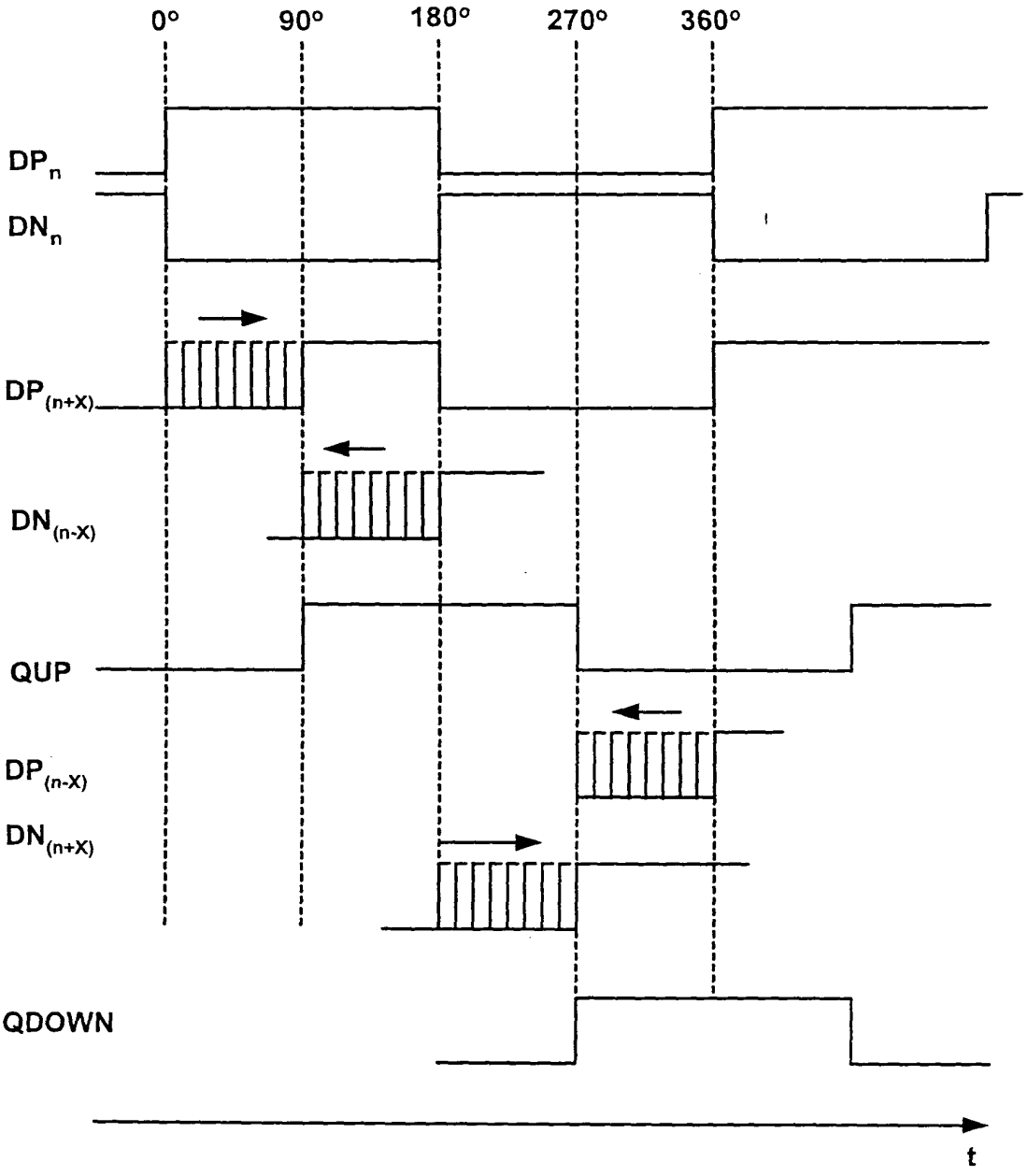
FIGURE 4


200
Q_CLK_OUT
260
Q
S
R
QUP
QDOWN
242
Q
D
DP(n+X)
DN(n-X)
CONTROL (n)
TEST
240
QUAD CONTROL
262
264
220
212
232
252
248
250
210
230
244
246
DP(n+X)
DN(n-X)
DP(n-X)
DN(n+X)
XDPCNTRL1
XDNCNTRL1
XDPCNTRL2
XDNCNTRL2
N
(DP)
(DN)

# FIGURE 5


250
START
252
SET X TO MINIMUM VALUE
254
GENERATE DP(n-X)
AND DN(n+X)
256
CHECK VALUE OF TEST
260
TEST=1
NO
262
INCREMENT X
YES
264
DECREMENT X
DONE

# FIGURE 6



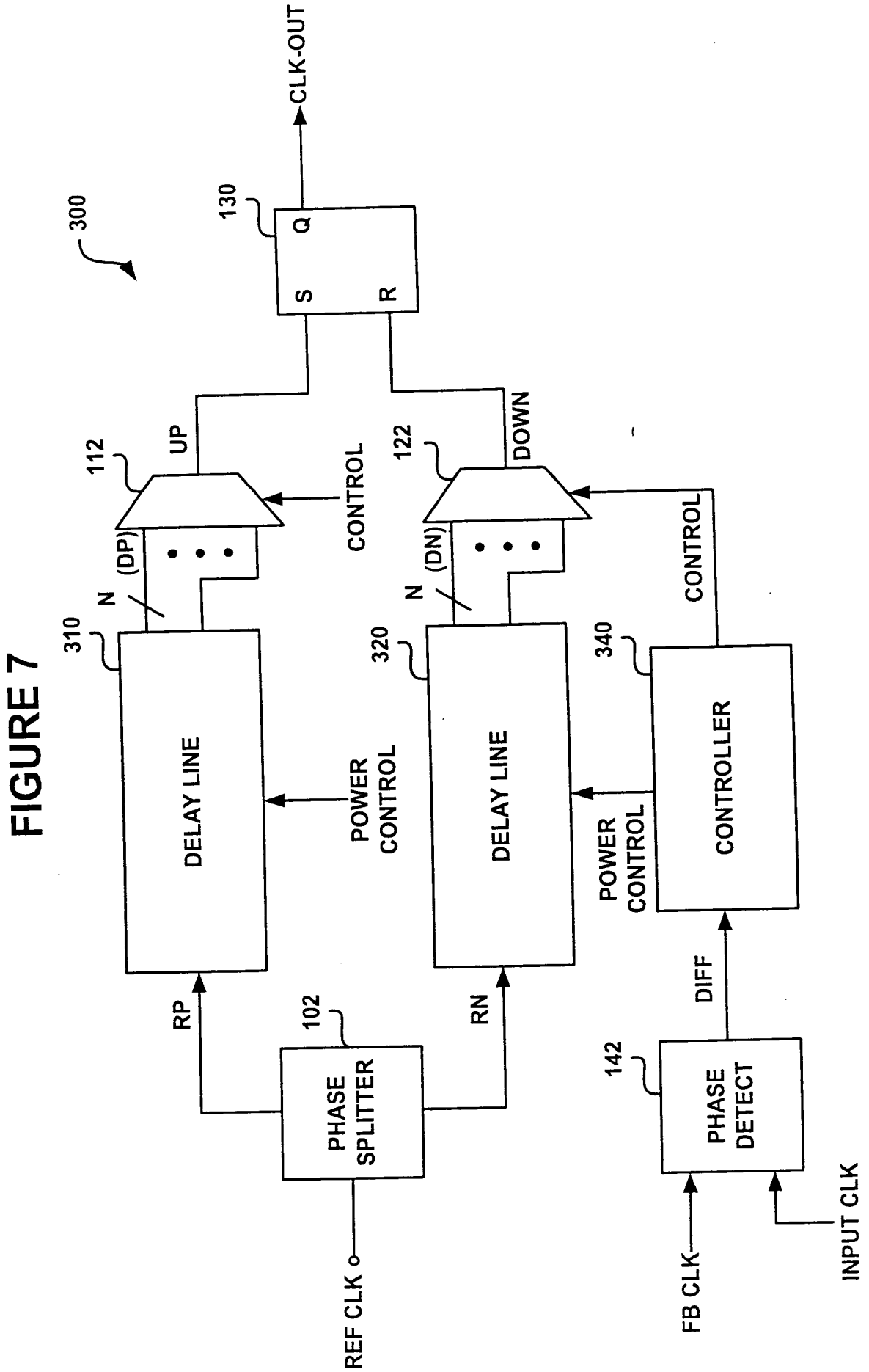
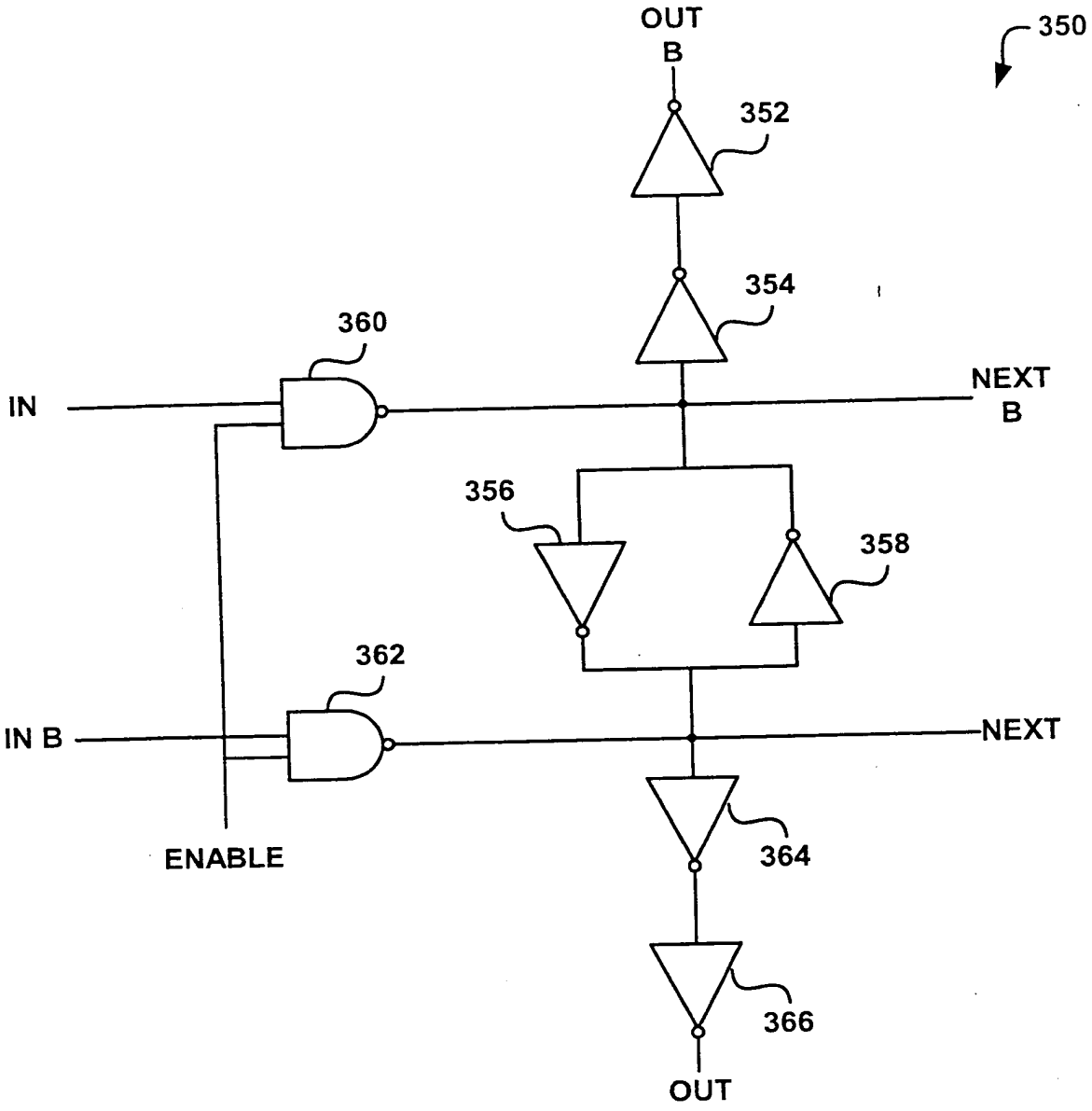

300
CLK-OUT
130
Q
S
R
112
UP
CONTROL
122
DOWN
N
(DP)
N
(DN)
CONTROL
310
320
340
DELAY LINE
POWER CONTROL
DELAY LINE
POWER CONTROL
CONTROLLER
RP
102
PHASE SPLITTER
RN
DIFF
142
PHASE DETECT
REF CLK
FB CLK
INPUT CLK

FIGURE 7

# FIGURE 8


OUT
B
350
352
354
360
IN
NEXT
B
356
358
362
IN B
NEXT
ENABLE
364
366
OUT

# FIGURE 9

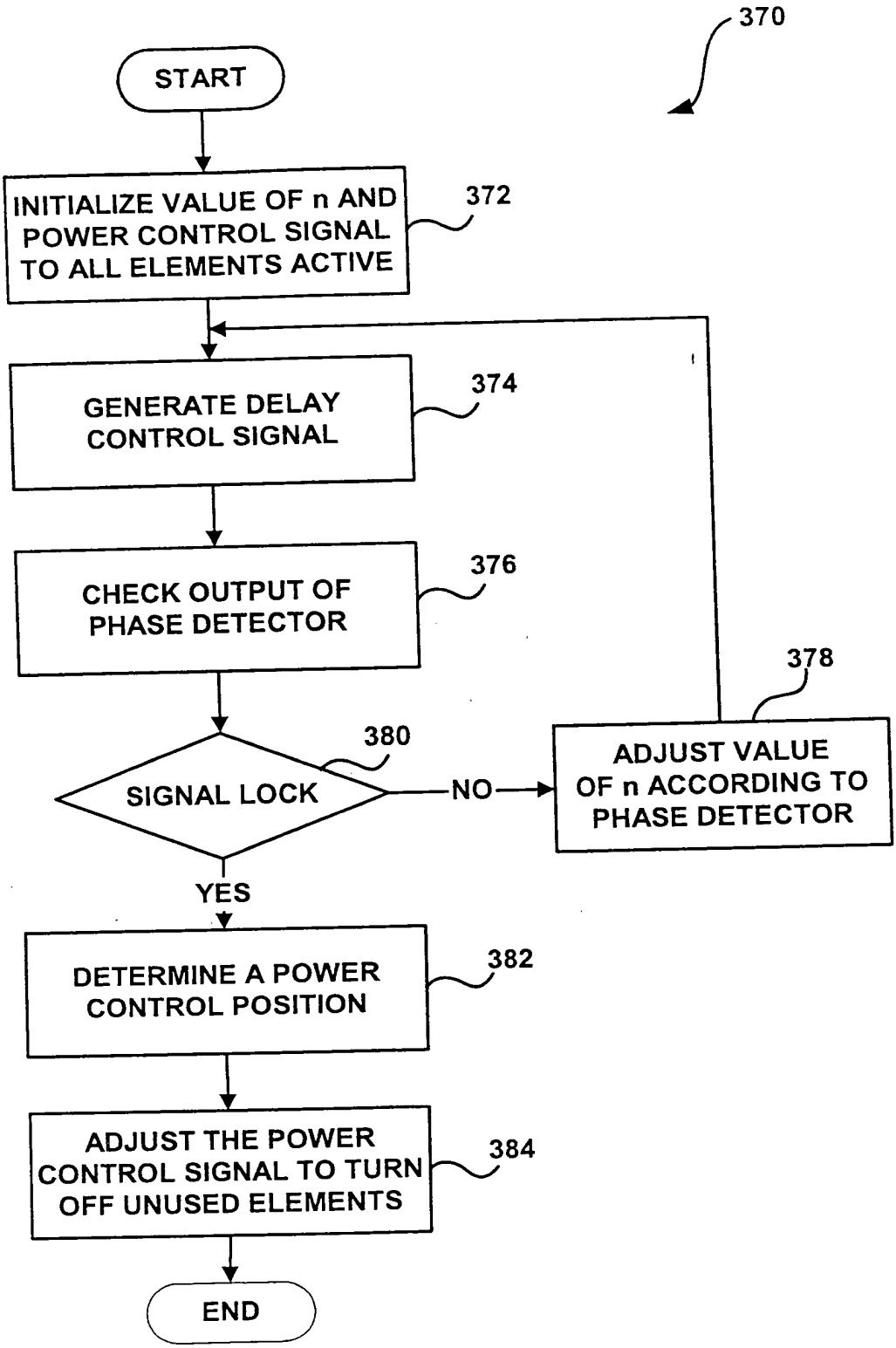
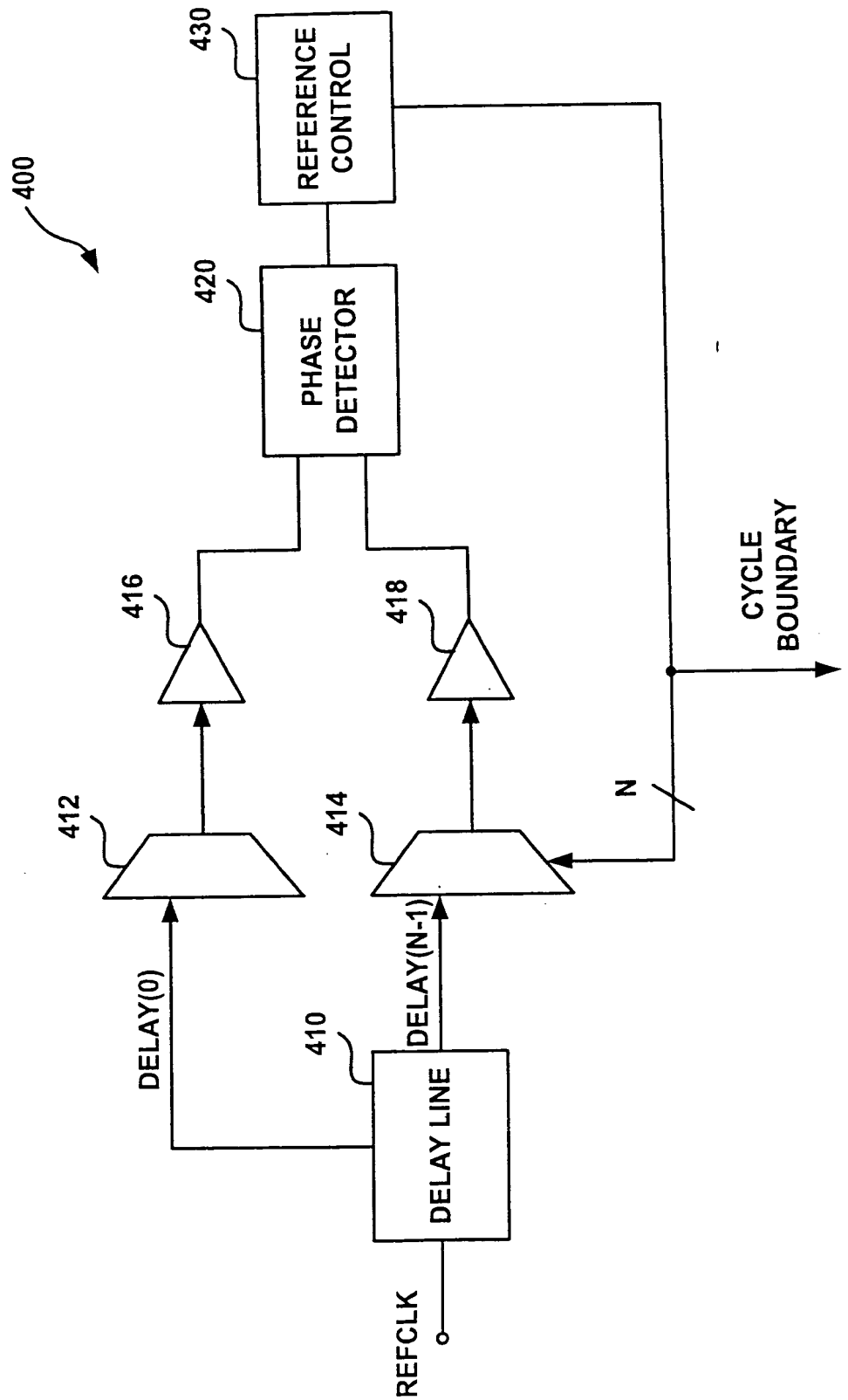
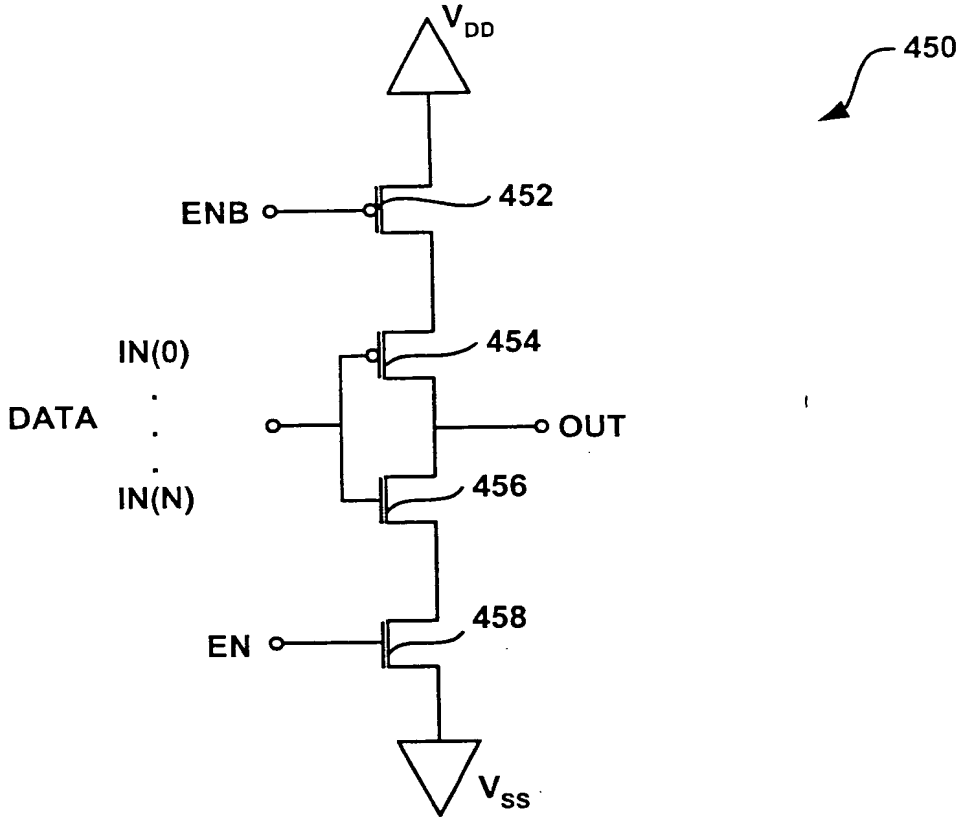

370
START
INITIALIZE VALUE OF n AND POWER CONTROL SIGNAL TO ALL ELEMENTS ACTIVE
372
GENERATE DELAY CONTROL SIGNAL
374
CHECK OUTPUT OF PHASE DETECTOR
376
SIGNAL LOCK
380
NO
ADJUST VALUE OF n ACCORDING TO PHASE DETECTOR
378
YES
DETERMINE A POWER CONTROL POSITION
382
ADJUST THE POWER CONTROL SIGNAL TO TURN OFF UNUSED ELEMENTS
384
END

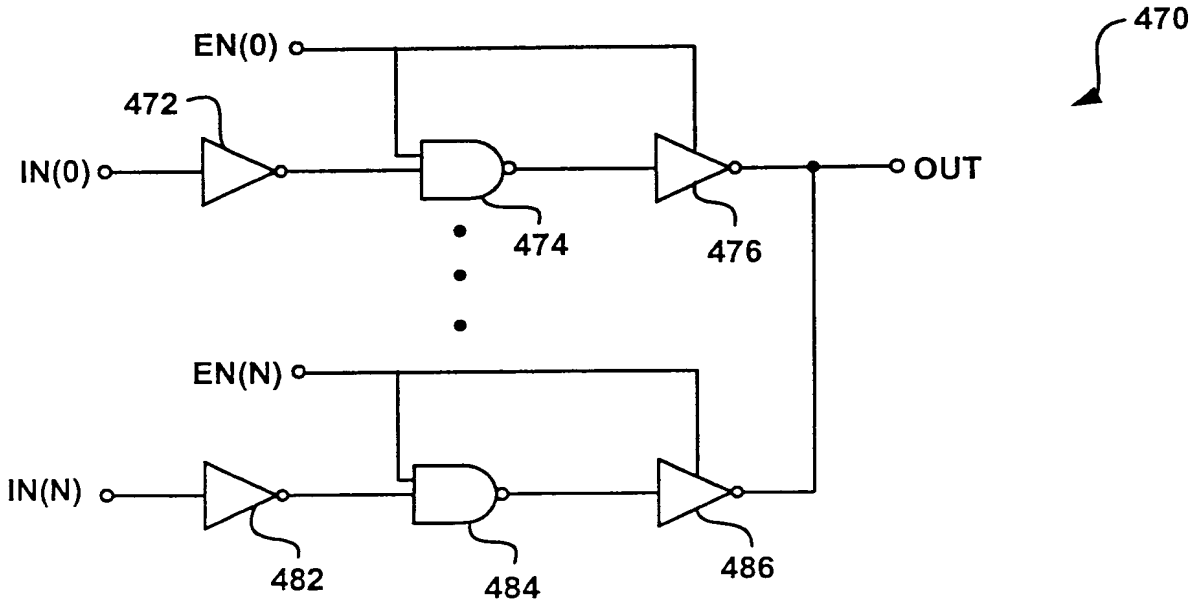
FIGURE 10


400
430
REFERENCE CONTROL
420
PHASE DETECTOR
416
418
CYCLE BOUNDARY
412
414
N
DELAY(0)
DELAY(N-1)
410
DELAY LINE
REFCLK

# FIGURE 11




# FIGURE 12



# FIGURE 13

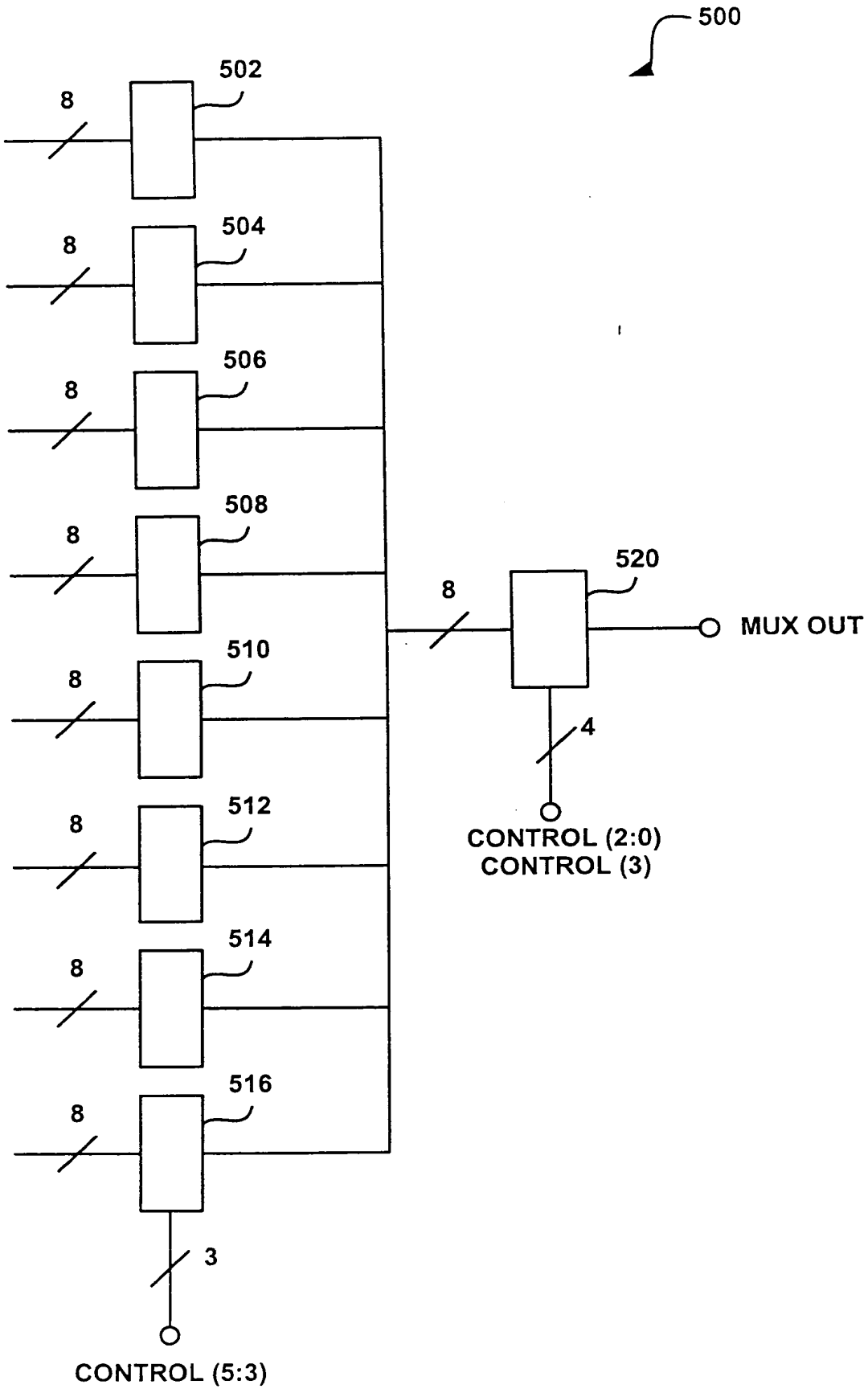
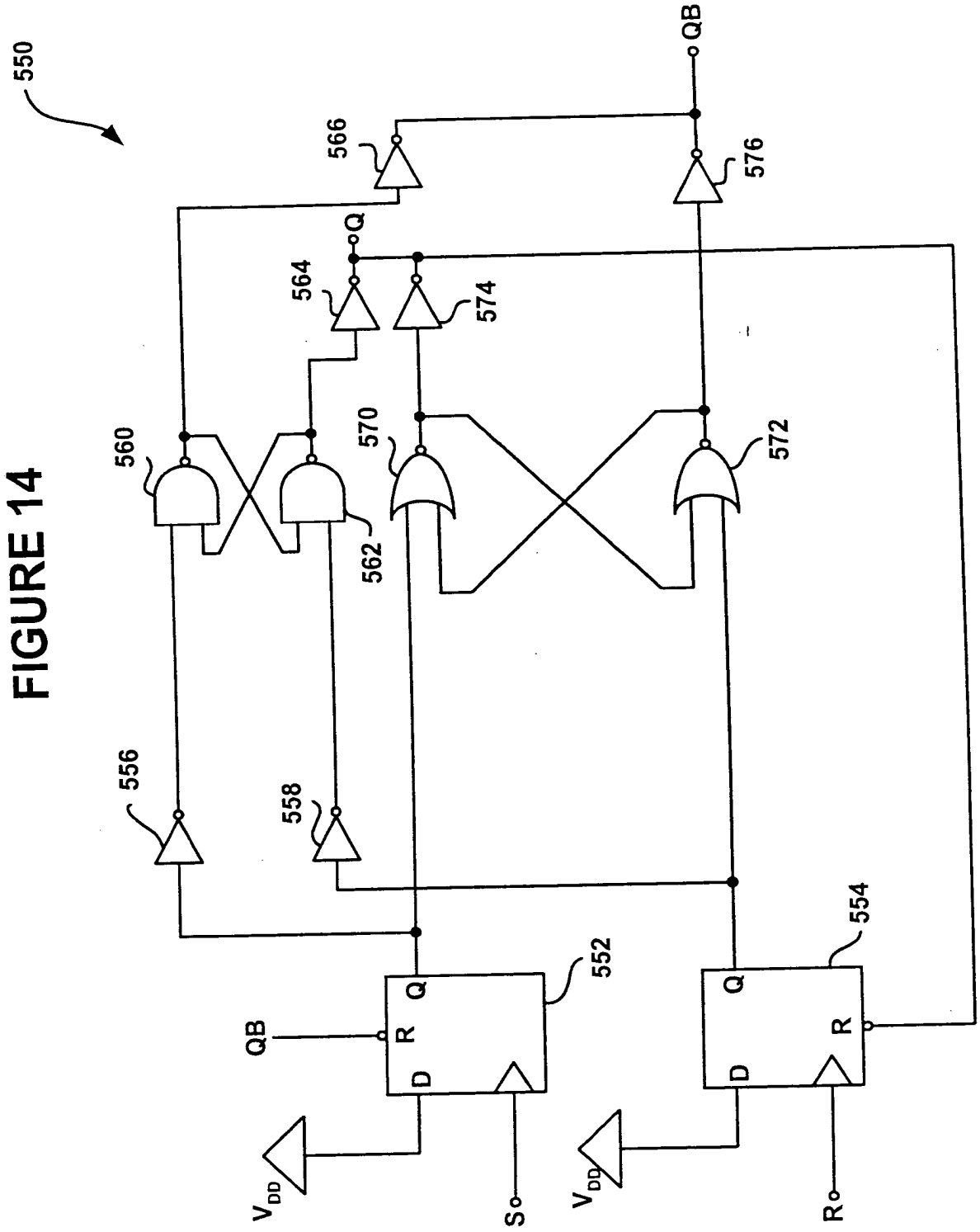

500
502
504
506
508
510
512
514
516
8
520
MUX OUT
4
CONTROL (2:0)
CONTROL (3)
3
CONTROL (5:3)

FIGURE 14


550
QB
566
576
Q
564
574
560
570
572
562
556
558
552
554
Q
R
D
QB
$V_{DD}$
S
R